Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A method of defining an opening in a stack of insulator layers on a semiconductor substrate, comprising the steps of:

providing a conductive region on said semiconductor substrate;

forming a tri-layer insulator composite on said conductive region and on portions of said semiconductor substrate;

forming an insulator layer on said tri-layer insulator composite;

forming an opening in said insulator layer to expose a portion of a top surface of said tri-layer insulator composite; and

removing portion of said tri-layer insulator composite exposed in said opening, exposing a portion of a top surface of said conductive region,

wherein said tri-layer insulator composite is comprised of an underlying silicon rich - silicon oxide layer, a hydro - silicon oxynitride (SiOxNH) layer, and an overlying silicon nitride layer.

2. (Previously Presented) The method of claim 1, wherein said conductive region is a source/drain region in a semiconductor substrate, a metal interconnect structure or a further metal structure.

3. (Cancelled)

4. (Currently Amended) The method of claim [[1]] 1, wherein said underlying silicon rich-silicon oxide layer of said tri-layer insulator composite, is formed via low pressure

chemical vapor deposition (LPCVD), via plasma enhanced chemical vapor deposition (PECVD), or via high density plasma chemical vapor deposition (HDPCVD) procedures, to a thickness between about 100 to 200 Angstroms, using silane or disilane, and oxygen or nitrous oxide as reactants.

5. (Previously Presented) The method of claim 1, wherein said underlying silicon rich-silicon oxide layer of said tri-layer insulator composite includes a refractive index between about 1.485 to 1.55.

6. (Previously Presented) The method of claim 1, wherein said hydro - silicon oxynitride (SiOxNH) layer is formed via LPCVD, PECVD, or HDPCVD procedures to a thickness between about 200 to 500 Angstroms.

7. (Previously Presented) The method of claim 1, wherein said overlying silicon nitride layer is formed via LPCVD or PECVD procedures to a thickness between about 100 to 200 Angstroms.

8. (Original) The method of claim 1, wherein said insulator layer is comprised of an underlying boro-phosphosilicate glass (BPSG) layer, obtained via PECVD or LPCVD procedures to a thickness between about 1500 to 2500 Angstroms.

9. (Original) The method of claim 1, wherein said insulator layer is comprised of an overlying silicon oxide layer, obtained via PECVD or LPCVD procedures to a thickness between about 5000 to 6000 Angstroms, using tetraethylorthosilicate (TEOS) as a source.

10. (Original) The method of claim 1, wherein said opening in said insulator layer is formed via a dry etch, anisotropic reactive ion etch (RIE) procedure, using CHF_3 as an etchant for said insulator layer.

11. (Original) The method of claim 1, wherein an over etch cycle used as a component of a dry etch procedure for said opening in said insulator layer, is performed via an anisotropic RIE procedure for a time between about 30 to 60sec, using CHF_3 as an etchant.

12. (Currently Amended) The method of claim 1, wherein said overlying silicon nitride layer is removed via an anisotropic RIE procedure using CF_4 or [[$C1_2$]] $\underline{Cl_2}$ as an etchant.

13. (Previously Presented) The method of claim 1, wherein said silicon rich-silicon oxide layer of said tri-layer insulator composite is removed via anisotropic RIE procedure using CHF_3 as an etchant.

14. (Previously Presented) A method of forming a opening in a stack of insulator layers located on an underlying conductive region, featuring a tri-layer insulator composite as an underlying component of the stack of insulator layers, used as a stop layer during an over etch cycle used to completely remove overlying components of said stack of insulator layers, comprising the steps of:

providing said conductive region;

forming said tri-layer insulator composite comprised of an underlying silicon rich-silicon oxide layer, a hydro - silicon oxynitride (SiOxNH) layer, and an overlying silicon nitride layer;

forming an overlying insulator layer;

forming photoresist shape with an opening exposing a portion of a top surface of said overlying insulator layer;

performing a first phase of a dry etch procedure to remove portions of said overlying insulator layer exposed in said opening in said photoresist shape;

performing an over etch cycle as a second phase of said dry etch procedure to insure complete removal of said overlying insulator layer, with said over etch cycle terminating at the top surface of said silicon nitride layer of said tri-layer insulator composite;

performing a third phase of said dry etch procedure to selectively remove exposed portions of said silicon nitride and of said SiOxNH; and

performing a fourth phase of said anisotropic dry etch procedure to selectively remove exposed portion of said silicon rich - silicon oxide layer, exposing a portion of a top surface of said conductive region.

15. (Original) The method of claim 14, wherein said conductive region is a source/drain region in a semiconductor substrate, or a metal structure such as a metal interconnect structure.

16. (Previously Presented) The method of claim 14, wherein said underlying silicon rich-silicon oxide layer is formed via low pressure chemical vapor deposition (LPCVD), or via plasma enhanced chemical vapor deposition (PECVD) procedures, to a thickness between about 100 to 200 Angstroms, using silane or disilane, and oxygen or nitrous oxide as reactants.

17. (Previously Presented) The method of claim 14, wherein said SiOxNH layer is formed via LPCVD or via PECVD procedures, to a thickness between about 200 to 500 Angstroms.

18. (Original) The method of claim 14, wherein said silicon nitride layer is formed via LPCVD or PECVD procedures, to a thickness between about 100 to 200 Angstroms.

19. (Original) The method of claim 14, wherein said overlying insulator layer is comprised of an underlying boro-phosphosilicate glass (BPSG) layer, obtained via PECVD or LPCVD procedures to a thickness between about 1500 to 2500 Angstroms, and comprised of an overlying silicon oxide layer, obtained via PECVD or LPCVD procedures to a thickness between about 5000 to 6000 Angstroms, using tetraethylorthosilicate (TEOS) as a source.

20. (Original) The method of claim 14, wherein said first phase of said dry etch procedure, employed to define said opening in said overlying insulator layer, is an anisotropic reactive ion etch (RIE) procedure performed using CHF_3 as an etchant for said overlying insulator layer.

21. (Original) The method of claim 14, wherein said over etch cycle of said second phase of said dry etch procedure, is an anisotropic RIE procedure performed for a time between about 30 to 60 sec., using CHF_3 as an etchant.

22. (Currently Amended) The method of claim 14, wherein said third phase of said dry etch procedure used to selectively remove said silicon nitride layer, is an anisotropic RIE procedure performed using CF_4 or ~~[[$C1_2$]]~~ $\underline{Cl_2}$ as an etchant.

23. (Previously Presented) The method of claim 14, wherein said fourth phase of said dry etch procedure used to selectively remove said silicon rich-silicon oxide layer, is an anisotropic RIE procedure performed using CHF_3 as an etchant.

24. (Currently Amended) A method of forming an opening in insulator layers, comprising the steps of:

providing a semiconductor substrate;

forming a conductive region directly on and contacting said semiconductor substrate;

forming a tri-layer insulator over said conductive region and on said semiconductor substrate, with said tri-layer insulator comprised with a hydro-silicon oxynitride (SiOxNH) middle layer;

forming an insulator layer directly on and contacting said tri-layer insulator; and

forming an opening in said insulator layer and in said tri-layer insulator to expose said conductive region.

25. (Original) The method of claim 24, wherein said conductive region is a source/drain region in a semiconductor substrate, or a metal structure such as a metal interconnect structure.

26. (Previously Presented) The method of claim 24, wherein said tri-layer insulator is comprised of an underlying silicon rich-silicon oxide layer at a thickness between about 100 to 200 Angstroms, comprised of said SiOxNH middle layer at a thickness between about 200 to 500 Angstroms, and comprised of an overlying silicon nitride layer at a thickness between about 100 to 200 Angstroms.

27. (Original) The method of claim 24, wherein said overlying insulator layer is comprised of an underlying boro-phosphosilicate glass (BPSG) layer at a thickness between about 1500 to 2500 Angstroms, and comprised of an overlying silicon oxide layer at a thickness between about 5000 to 6000 Angstroms.

28. (Original) The method of claim 24, wherein said opening in said insulator layer and in said tri-layer insulator is formed via a dry etch, anisotropic reactive ion etch (RIE) procedure.